ECE 526L

Lab 2 Report

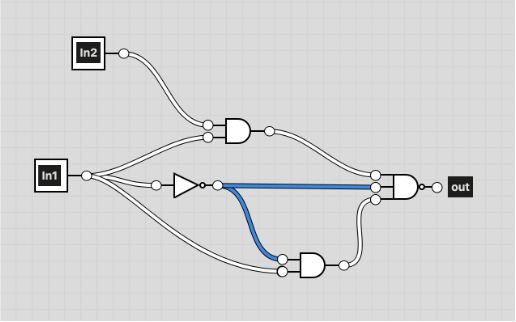
By

Avinash Damse

CSUN ID- 203131064

**1: Introduction**

The objective of this lab is to build a below circuit with two inputs and one output using AND, NOT and NAND gates which uses delays for primitives. And changing the delays later on to see how it affects the waveforms.



Here initially all the delays are 0 ns.

### **Truth table**

The truth table of the given circuit is given below for given test cases . Here we are using two inputs(In1,In2) which produces one output (out).

|  |  |  |
| --- | --- | --- |
| In1 | In2 | out |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**2: Procedure**

**a. Part 1: Creating Lab2\_1 Module**

In this lab I have created a module given circuit . Inside the module I have assigned “In1”,”In2” as input variables and “out” as output variables. Then I performed “AND”,”NOT” and “NAND” operations. According to the circuit given in the diagram . After completing the code I ended the module using and saved the file with name “Lab2\_1.v”.

**b. Part 2: Creating Lab2\_1\_tb Module**

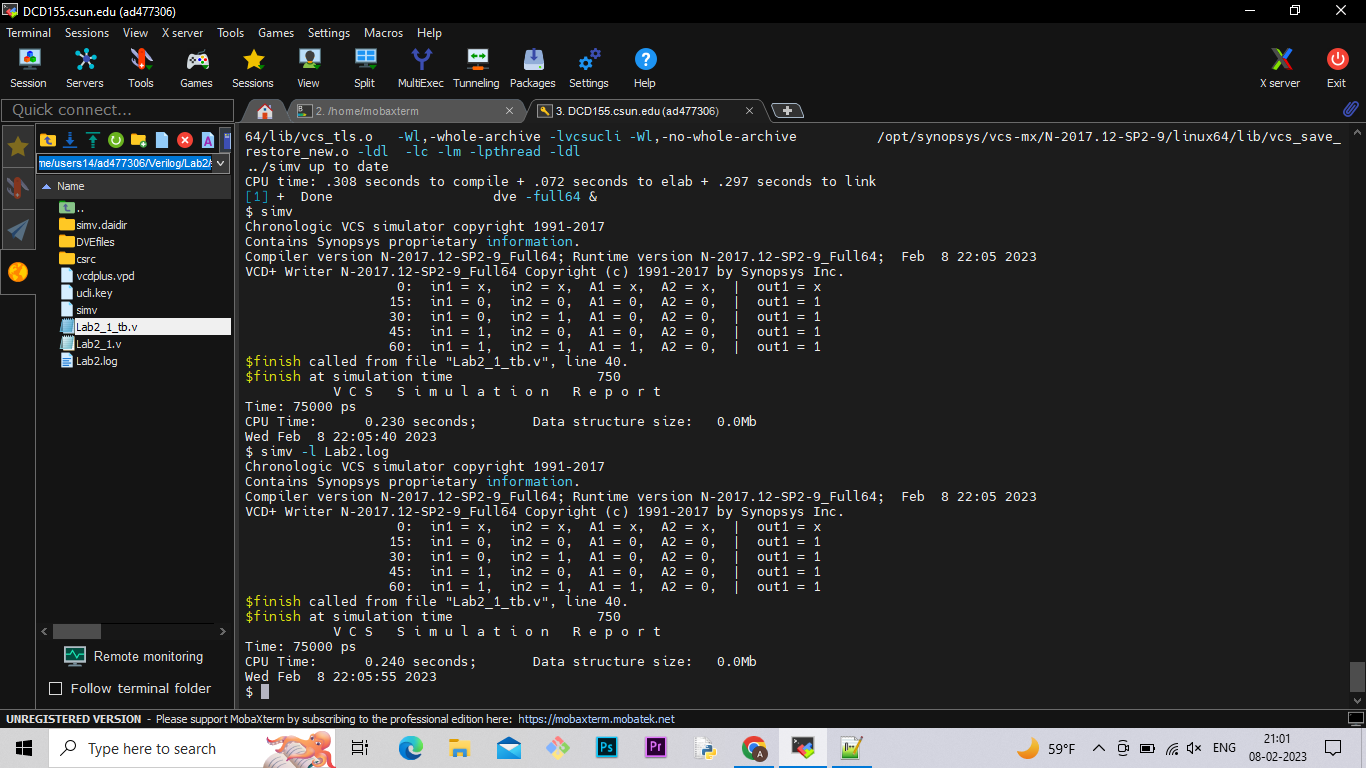
I have written the testbench for the Lab2\_1 module code after creating my module. We require testbench just to make sure that the module we have created is working properly. In this lab, I have written the testbench and saved the file as “Lab2\_1\_tb.v”.

**c. Part 3: Checking the Lab2\_1 and Test Bench Module**

After completing the Lab2\_1 module and testbench module , we have to check if the code is running properly or not. To make sure that the code is running perfectly or not I have run the VCS command followed by the Lab2\_1.v and Lab2\_1\_tb.v module. I have used the command “vcs -debug -full64 Lab2\_1.v Lab2\_1\_tb.v” and checked if any error occurs. I found one error in the code, with the help of the “gedit” command. I edited the code and re-run again. This time code executed without any error.

**d. Part 4: Simulation**

After completing the code and testbench for Lab2\_1 I have run the command “simv” for simulation.

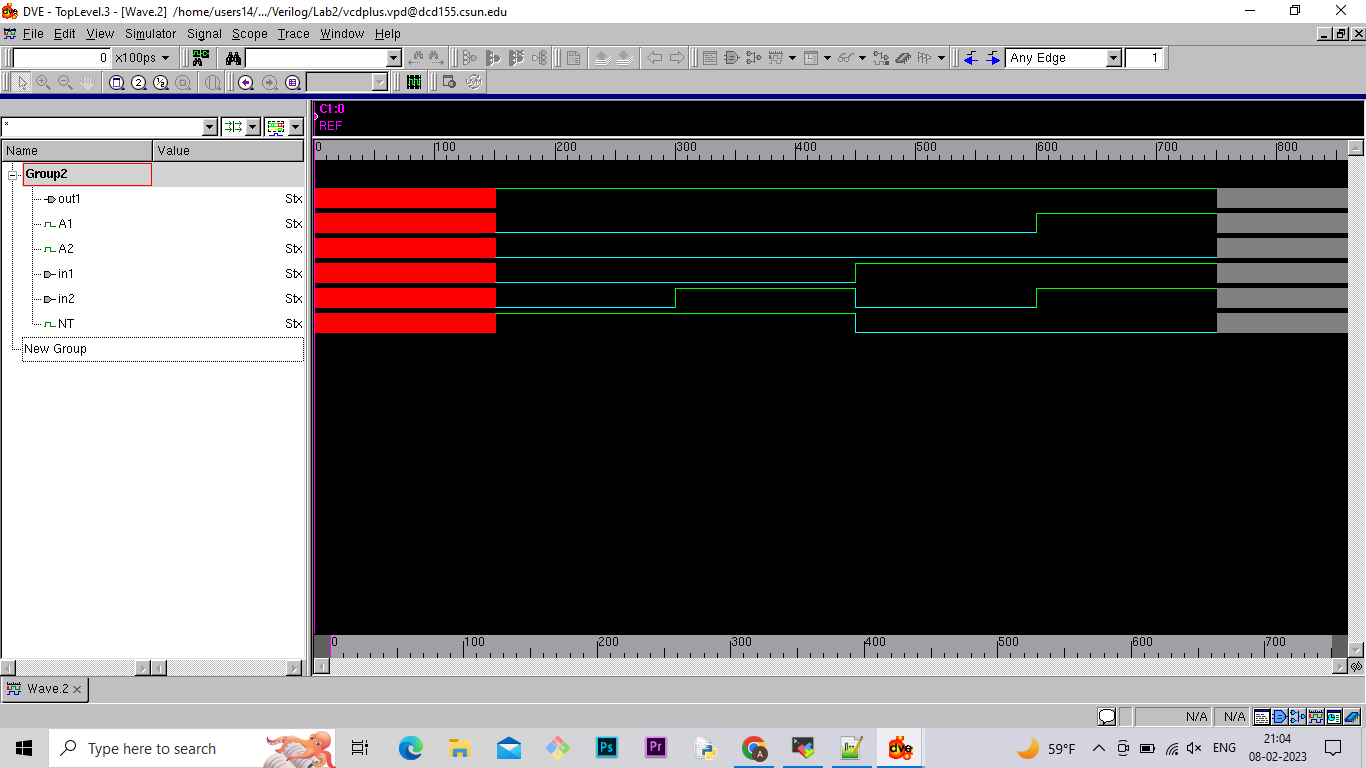
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**e. Part 5: Creating Log File**

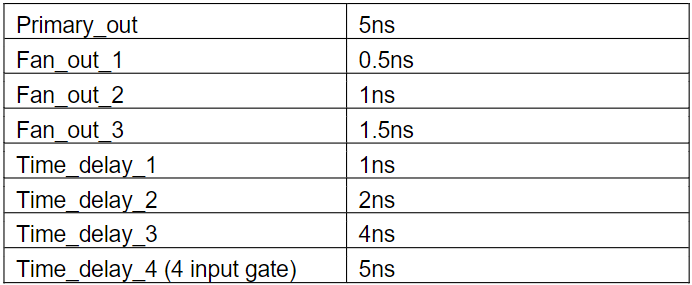
After running the simulation I created the log file using the “simv -l Lab2.log” command.

**f. Part 6: Seeing the waveform.**

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveform.



**Part 2 With Changes in delays.**

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Here I repeated all the steps I did in the first part without delays. And the results i got are as follows:

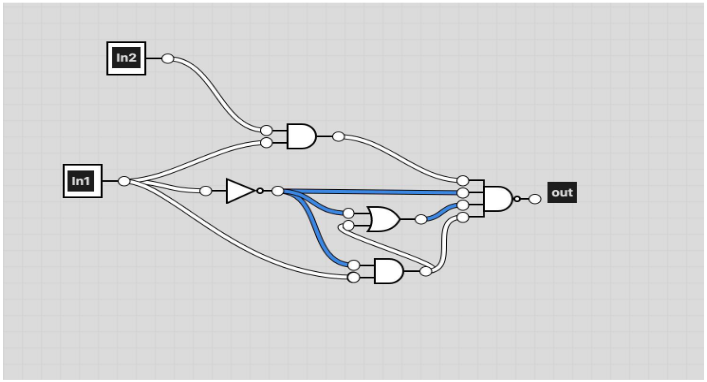
**Simulation :**

**Waveform :**

**Lab report question: What’s the critical path (longest delay) of this**

**design?**

**Part 3 : New Circuit**

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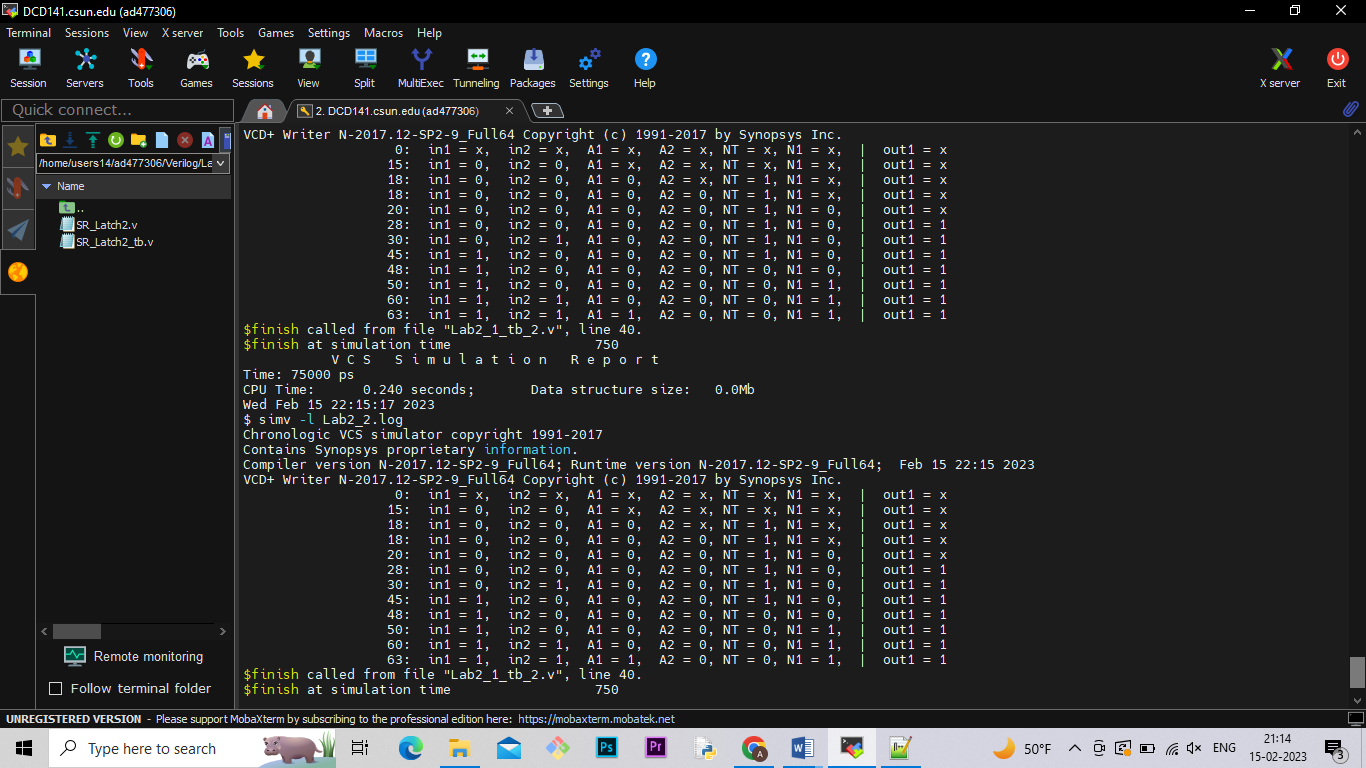
Here in the new circuit there is addition of one NOR gate which takes inputs from the previous AND(A2) and NOT(NT) gate which will be further added to the final NAND gate to get output.

### **Truth table**

The truth table of the new circuit is given below for given test cases . Here we are using two inputs(In1,In2) which produces one output (out1).

|  |  |  |
| --- | --- | --- |
|  |  |  |
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|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

**Simulation :**

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**Waveform :**

**Lab report question: What’s the critical path (longest delay) of this new**

**design?**

**Conclusion :**

In this lab I learned how to design circuit diagrams with given inputs and some gates in verilog . This lab taught me how to calculate the longest delay in any circuit diagram . And how slight change in the delays changes the waveforms.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed) Date : 14-02-2023

